

Controllable p–n Switching Behaviors of GaAs Nanowires *via* an Interface Effect

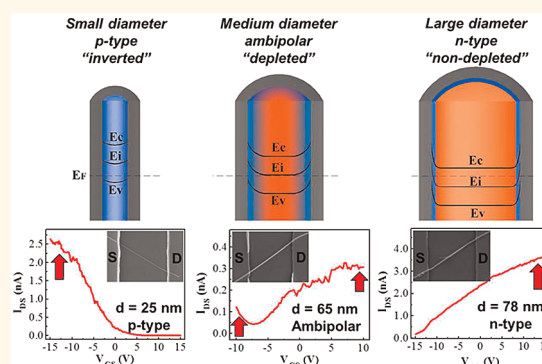
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Due to the unique electronic and optical properties, III–V compound semiconductor nanowire (NW) materials such as gallium arsenide (GaAs) and indium arsenide (InAs) have been extensively explored for versatile device applications.^{1–6} Among these, NW field-effect transistors are the fundamental elements in pursuing next-generation nano-electronics; therefore, it is important to understand the electronic transport properties of these transistors. Of particular interest is the ability to control the atomic composition of these NW channels; especially, the modulation between p- and n-type conduction is highly attractive for enabling the NW complementary metal-oxide-semiconductor (CMOS) technology. Conventional route for achieving such control is the *in situ* doping during NW growth which relies on good control of complex process parameters such as the vapor pressure of dopants, V/III ratio, growth temperatures, and others.^{7,8} On the other hand, the post-growth ion implantation still suffers from the incompatibility with NWs and severe crystal damage.^{9,10} To overcome the difficulties of conventional technologies, tremendous efforts have been taken in recent years to develop new techniques to tailor electronic transport properties of NWs by modulating the channel conduction.^{11–16}

Recently, Li *et al.* have prepared InAs/InP core/shell NWs with small diameters and heavily doped the InP shell with Zn. The p-type InP shell would then induce an interface depletion of all electrons in the InAs core to achieve efficient p-type conduction in InAs NWs,¹⁷ which is known to be difficult due to the surface Fermi level pinning of InAs in the conduction band.¹⁸ Also, Hong *et al.* have reported the surface morphology and size-dependent tunable electronic

ABSTRACT



Due to the extraordinary large surface-to-volume ratio, surface effects on semiconductor nanowires have been extensively investigated in recent years for various technological applications. Here, we present a facile interface trapping approach to alter electronic transport properties of GaAs nanowires as a function of diameter utilizing the acceptor-like defect states located between the intrinsic nanowire and its amorphous native oxide shell. Using a nanowire field-effect transistor (FET) device structure, p- to n-channel switching behaviors have been achieved with increasing NW diameters. Interestingly, this oxide interface is shown to induce a space-charge layer penetrating deep into the thin nanowire to deplete all electrons, leading to inversion and thus p-type conduction as compared to the thick and intrinsically n-type GaAs NWs. More generally, all of these might also be applicable to other nanowire material systems with similar interface trapping effects; therefore, careful device design considerations are required for achieving the optimal nanowire device performances.

KEYWORDS: gallium arsenide (GaAs) nanowires · diameter-dependent · tunable electronic transport · p–n conduction switching · interface trapping effect

transport properties of ZnO NWs.¹⁹ By tuning the surface roughness and NW diameters, the threshold voltages of fabricated NW FETs can be controlled to result in depletion-mode *versus* enhancement-mode device operation. Therefore, optimum control of the NW surface and/or interface states is an important factor in controlling their corresponding device

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properties.^{20–29} Here, we present a facile and reliable approach to tailor the electronic transport properties of GaAs NWs utilizing the abundant acceptor-like interface trapping states located between the intrinsic GaAs core and its amorphous oxide shell. For the large diameters ($d > 70$ nm), only a shallow space-charge depletion results from the oxide shell (trap states) to give intrinsic n-channel conduction of GaAs NWs, whereas for the smaller diameters ($d < 40$ nm), due to the enhanced surface-to-volume ratio, the contribution coming from the oxide trap states becomes more pronounced and yields fully depleted NWs to exhibit trap-state-dominant and inverted p-channel behavior. Ambipolar conduction in lower current magnitude is observed for the NW diameters between $40 < d < 70$ nm, and by further oxidizing such NWs to enhance the carrier depletion, the conductivity of GaAs NWs can be controlled accordingly.

RESULTS AND DISCUSSION

GaAs NWs used in this study were synthesized using a catalytic solid-source chemical vapor deposition (CVD) method similar to the ones previously reported.³⁰ In brief, during the growth, Au nanoparticles were used as catalysts and obtained by the thermal annealing (~ 800 °C for 10 min) of a predeposited 2.5 nm thick evaporated Au layer on the 50 nm thick Si/SiO₂ substrates. The subsequent growth temperatures, both source and substrate zones, as well as flow rate of carrier gas, H₂, were carefully adjusted to control the physical properties of NWs. After a detailed growth investigation, the growth condition was optimized with the source temperatures of 900–925 °C, substrate temperatures of 590–610 °C, and gas flow rates of 100–200 sccm. As shown in Figure 1a, the grown GaAs NWs are over 10 μ m long with a diameter range of 39 ± 8 nm (Figure S1c in the Supporting Information) and a

high growth density. The NWs are single crystalline in the zinc blende structure with a dominant growth axis in the $\langle 111 \rangle$ direction, as evidenced from X-ray diffraction (XRD) and transmission electron microscopy (TEM) analysis (Figure 1b–d). This preferential growth direction is expected due to the lowest free surface energy in $\{111\}$ planes of cubic III–V NW materials. In addition, the presence of spherical catalytic tips further confirms the vapor–liquid–solid/vapor–solid–solid (VLS/VSS) growth mechanism in this CVD technique, as depicted in Figure 1c. Importantly, the NWs do not exhibit any noticeable tapering effect with a uniform length of each NW and a uniform native oxide thickness of 3–4 nm (Figure 1d). Jabeen *et al.* have experimentally found that this oxide shell would deplete the carrier density in GaAs NWs by contributing abundant acceptor-like interface trapping states and/or defects, in which the depletion space-charge region can extend deep inside the NWs.²² In this regard, the penetration of this oxide-induced space-charge region could be further manipulated by varying the NW diameter in order to tailor the electrical properties of GaAs NWs in this investigation.

In order to study the effect of such interface trapping states on the electronic transport properties of GaAs NWs, we have examined the electronic transport characteristics using the NW FET structure configured in the global back-gated geometry with the NW channel of different diameters, as depicted in Figure 2. In this work, by changing the film thickness of Au catalyst deposited (0.5–12 nm), the size of nanoparticles can be controlled in the annealing process, which leads to the NWs grown with different diameters.⁴ More than 100 NWs were analyzed from TEM images to statistically determine the diameter distribution of each

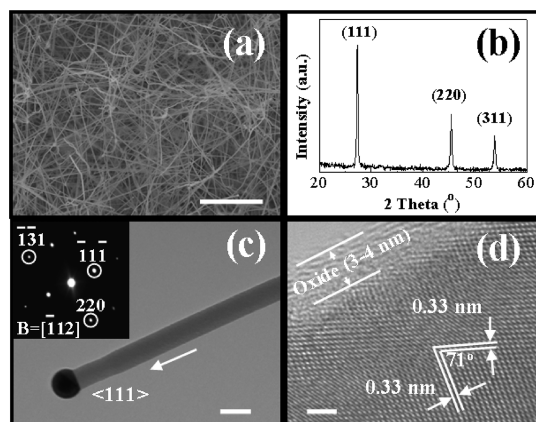


Figure 1. Morphology and structural characterization of GaAs NWs prepared by the 2.5 nm thick thin-film Au catalyst: (a) SEM image (scale bar = 2 μ m) and (b) XRD pattern of the NWs grown on Si/SiO₂ substrate, (c) TEM image (scale bar = 50 nm) and SAED pattern of one representative NW showing the $\langle 111 \rangle$ growth direction, and (d) HRTEM image (scale bar = 2 nm) of the NW in (c).

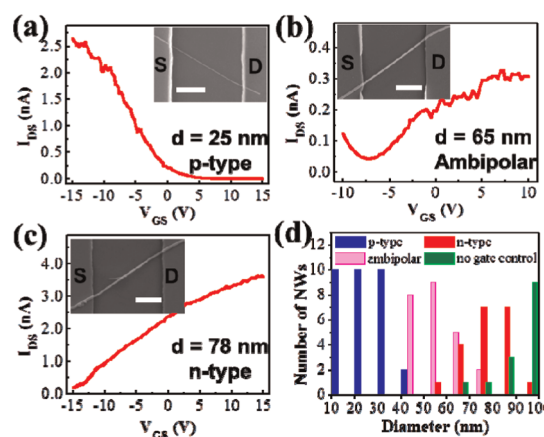


Figure 2. Typical I_{DS} – V_{GS} curves of GaAs NW FETs based on different NW diameters ($V_{DS} = 2$ V): (a) p-type characteristic ($d = 25$ nm), (b) ambipolar conduction ($d = 65$ nm), (c) n-type characteristic ($d = 78$ nm), and (d) statistics of the p- to n-type transition with increasing NW diameters in the range of 10–100 nm, with 10 NWs in each 10 nm increment. The insets are the SEM images of the corresponding GaAs NW devices (scale bar = 1 μ m).

starting Au film thickness (see Supporting Information Figure S1). Figure 2a shows the representative p-type electrical property of a GaAs NW with a small diameter (~ 25 nm) and an ON current of ~ 2.5 nA ($I_{\text{ON}}/I_{\text{OFF}} > 10^3$). However, instead of enlarging the p-type ON current, when the diameter increases, the p-type characteristic diminishes to yield ambipolar conducting behavior in the lower current magnitude (Figure 2b) and eventually the n-channel behavior is obtained (Figure 2c). When the diameter is greater than 90 nm, the NW channel can no longer be controlled by the gate due to the inefficient gate coupling in the back-gated configuration, exhibiting metallic-like conduction (see Supporting Information Figure S2). At the same time, more than 90 NWs are statistically summarized in the diameter range of 10–100 nm, with 10 NWs in each 10 nm increment, as shown in Figure 2d, which clearly show the consistent data trend. Notably, no impurity is intentionally introduced during the NW growth, and all NWs are grown using the same CVD system with the same residual impurity level. Also, the device fabrication is performed under the same condition among all devices. All of these indicate the well-controlled p–n switching of GaAs NWs by just only tailoring the diameters (Figure 2d). In this case, NW diameters are experimentally shown to have a significant effect on the intrinsic electronic transport properties of NW-based devices.

To further understand the physical mechanism of this p–n switching, Figure 3 shows cross-sectional schematics along the NWs with different diameters with the corresponding equilibrium energy band diagram at zero gate bias. Specifically, as discussed above, the native oxide shell would contribute the acceptor-like interface trapping states depleting electrons in the NWs and result in the band bending.^{20,31} In contrast to the Fermi level pinning, this space-charge depletion layer thickness depends on the NW diameter.^{16,32} For the thin NWs, because of the extremely high aspect ratio (large surface-to-volume ratio), the depletion region extends over the entire volume of NWs to yield the energy bands high up with respect to the Fermi level (E_F), leading to inversion and p-type conduction along the acceptor-like oxide/NW interface trapping states (Figure 3a). When the NWs become thicker, the depletion layer cannot completely extend into the bulk of NWs, namely, just depleted and an electron conduction channel in the NW core is present. In this case, the energy bands would not bend as much to have the E_F located in the middle of the band contributing the ambipolar behavior in the lower current level (Figure 3b). In the extremely thick NW case, the depletion layer is only confined in the outermost shell of the NW, whereas the electron conduction channel becomes dominant and demonstrates the intrinsically n-type conduction of GaAs NWs (Figure 3c).³³ All of these illustrate that the Fermi level is pinned at the

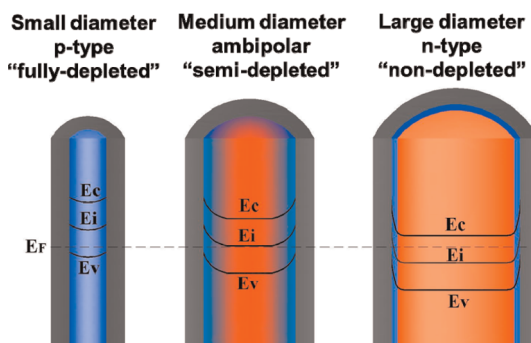


Figure 3. Cross-sectional view of GaAs NWs with different diameters and the corresponding equilibrium energy band diagram at zero gate bias. Each NW composes a NW core and an oxide shell.

oxide interface surface resulting in internal electric fields and in full depletion to inversion of NWs below a critical diameter ($d_c \sim 40$ – 70 nm) in order to reveal the p–n conduction switching. In order to confirm the existence of full depletion to inversion of NWs at a critical radius, the total number of charges existing in the NWs can be compared to the geometrical diameter. On the basis of the space-charge model, the GaAs NWs are believed to be intrinsically n-type,^{25,33} with the total number of donor concentration, N_D , proportional to $\pi r^2 L$, while the acceptor-like interface states would contribute to an acceptor concentration, N_A , proportional to $2\pi r L$, assuming a uniform distribution of space charge within the entire volume of the NW (where r is the radius and L is the length of the NW). In this case, due to the different dependence on the NW dimension, for the large NW diameter, the donor charges are dominant and yield n-channel behavior of the thick NWs. When the diameter decreases, donors and acceptors would cancel out each other at a critical radius (r_c), achieving the fully depleted and ambipolar conduction with the low current level. Eventually, for the smaller diameter ($< r_c$), acceptor charges become the majority and this way lead to the p-channel (see Supporting Information Figure S3). Using the equation $W = (2\epsilon\phi/eN)^{0.5}$, where W is depletion layer thickness, ϵ is the dielectric constant of GaAs (~ 13.1), ϕ is the surface barrier potential, e is the electronic charge, and N is the carrier density, a thickness of ~ 15 – 30 nm in the depletion layer thickness can be determined by estimating the surface potential of 0.1 – 0.2 eV and approximating the carrier concentration of 10^{17} – $10^{18}/\text{cm}^3$ in the NWs (see Supporting Information Figure S3).³⁴ All of these have further confirmed the small diameter NWs which could be fully depleted with these interface trapping states. It is also noted that this space-charge model is qualitative, and a more thorough theoretical model is required to further quantify the layer thickness of space-charge depletion with different NW diameters and evaluate the corresponding carrier concentration for electronic transport characteristics in the future.

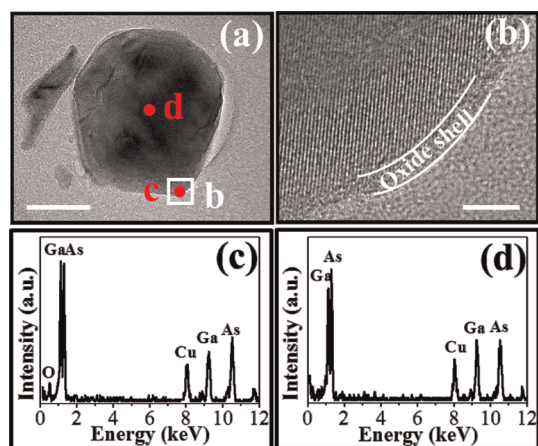


Figure 4. Radial cross-sectional TEM and HRTEM images of (a) 120 nm diameter NW (scale bar = 50 nm), (b) HRTEM image (scale bar = 5 nm) of spot b in (a), (c) EDS spectrum of spot c (NW shell), and (d) EDS spectrum of spot d (NW core).

On the other hand, in order to further ensure this p–n switching mechanism due to the oxide interface trapping states, the radial structures of NWs are characterized by high-resolution TEM and EDS, as shown in Figure 4. It is found that the NW core is highly crystalline and stoichiometric with a Ga/As ratio close to 1:1 (Figure 4b,d), suggesting the excellent crystal quality and good control of the growth process of GaAs NWs performed in this study. Also, an amorphous oxide shell is observed with a uniform thickness of 3–4 nm (Figure 4b,c), and importantly, this oxide layer thickness is independent of the NW diameter as compared to Figure 1d. More TEM and EDS analysis is performed on NWs with different diameters, and consistent results are obtained with the crystalline stoichiometric NW cores surrounded with uniform oxide shells (see Supporting Information Figure S4). All of these would further illustrate the existence of a uniform oxide shell (~3–4 nm) around NWs contributing abundant acceptor-like trap states to deplete carriers in the NW core.

To shed light on manipulating the electronic transport of GaAs NWs *via* these trap states, low-temperature ambient oxidation (25 °C for ~2500 h) is performed on these NWs in order to achieve their equilibrium oxide thickness, and their corresponding electrical performance is characterized. As demonstrated in Figure 5a, the thin NW loses its p-channel features after oxidation. When the oxide shell becomes thicker or an entire NW is oxidized, there are no acceptor-like interface states for the efficient electronic transport and the NW behaves like an insulator. For the thicker NWs, the n-type characteristic gets suppressed while the p-type conduction becomes more obvious (Figure 5b,c). It is due to the fact that the thicker oxide shell contributing a deeper space-charge region would deplete more electrons from the NW core to switch

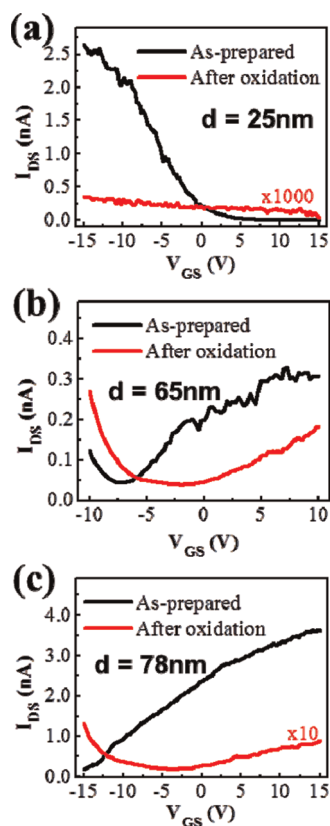


Figure 5. I_{DS} – V_{GS} curves of GaAs NW FETs under $V_{DS} = 2$ V as-prepared (black curves) and after ambient oxidation (red curves): (a) p-type FET changed into insulator, (b) n-type dominated ambipolar FET changed into p-channel dominated ambipolar behavior, and (c) n-type FET changed into ambipolar characteristic.

the n-type features to become more p-type dominant (see Supporting Information Figure S5). All of these agree well again with the proposed qualitative space-charge model to control the p–n switching behaviors of GaAs NWs *via* the manipulation of the oxide/NW interface trapping states. It is also noted that the diameter scaling of NWs not only affects their carrier mobility and gate coupling efficiency but also alters their electronic transport *via* the different contribution of the native-oxide-induced space-charge depletion; therefore, careful device design considerations are required for achieving the optimal device performances.

CONCLUSIONS

In summary, an approach to tailor the electronic transport properties of GaAs NWs utilizing the interface trapping states between the intrinsic GaAs core and its amorphous oxide shell is presented. Specifically, these acceptor-like trap states induce a space-charge depletion layer extending into the NW; as a result, the Fermi level is pinned at the oxide/NW interface surface, resulting in internal electric fields and in full depletion to inversion of NWs below a critical diameter (~40–70 nm), illustrating the p–n switching behaviors

in the electrical characterization of fabricated NW FETs. In the future, this controllable scheme can also be

applied to the other III–V NW material systems for technological applications.

METHODS

Nanowire Synthesis. A dual-zone horizontal tube furnace, one zone for the solid source (upstream) and one zone for the sample (downstream), was used as the reactor for the synthesis of GaAs NWs. At first, thermal evaporation was carried out with 99.995% pure Au particle to deposit 0.5, 2.5, 4.0, 6.0, and 12.0 nm thick Au films on Si/SiO₂ substrates (50 nm thermal grown) under a vacuum of $<5 \times 10^{-6}$ Torr. The processed substrate was then placed in the middle of the downstream zone with a tilt angle of $\sim 20^\circ$ and thermally annealed at 800 °C for 10 min in a hydrogen environment to obtain Au nanoclusters as the catalysts, similar to the technique reported in refs 4 and 11. The solid source, GaAs powders (99.9999% purity) placed within a boron nitride crucible, was positioned in the upstream zone with a distance of 10 cm away from the sample. During the NW growth, the source was heated to the required source temperature (900–925 °C) while the substrate was cooled to the preset growth temperature (590–610 °C). Hydrogen (99.9995% purity) was used as the carrier gas to transport the thermally vaporized solid GaAs source to the downstream, and the pressure was maintained at ~ 1 Torr for the entire duration of the growth. After the growth, the source and substrate heater were stopped together and cooled to room temperature under the hydrogen flow. In this case, the NWs were grown chemically intrinsic without any intentional dopants.

Characterization of GaAs NWs. Surface morphologies of the grown NWs were examined with a scanning electron microscope (SEM, FEI/Philips XL30) and transmission electron microscope (TEM, Philips CM-20). Crystal structures were determined by collecting X-ray diffraction (XRD) patterns on a Philips powder diffractometer using Cu K α radiation ($\lambda = 1.5406$ Å), imaging with high-resolution TEM (JEOL 2100F) and selected area electron diffraction (SAED, Philips CM-20). Elemental mappings were performed using an energy-dispersive X-ray spectrometry (EDS) detector attached to the JEOL 2100F to measure the chemical composition of grown NWs. For the elemental mapping and TEM, the GaAs NWs were first suspended in the ethanol solution by ultrasonication and drop-casted onto the grid for the corresponding characterization. For the cross-sectional HRTEM observation, the GaAs NWs were dispersed in resin, which was cut into ~ 25 nm slices after dried and supported by a copper grid.

GaAs NW FET Fabrication and Characterization. GaAs NW FETs were fabricated by drop-casting the NW suspension onto highly doped p-type Si substrates with a 50 nm thermally grown gate oxide. Photolithography was utilized to define the source and drain regions with a 2 μ m channel using a AZ5206E photoresist, and 50 nm thick Ni was thermally deposited as the contact electrodes followed by a lift-off process. Electrical performance of fabricated back-gated FETs was characterized with a standard electrical probe station and Agilent 4155C semiconductor analyzer.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: GaAs NW diameter distribution grown with different thickness of Au catalysts; electrical characterization of NW FETs with different NW diameters as channels; qualitative space-charge model; scanning TEM and EDS analysis in the radial cross section of GaAs NWs with different diameters; corresponding electrical characterization of NW FETs after oxidation. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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